What is claimed is:

1. An electrostatic discharge protection circuit comprising:

one or more electrostatic bus lines to direct electrostatic discharge around internal circuitry;

a plurality of signal bonding pads to receive external voltage signals, each signal bonding pad is coupled to an associated electrostatic bus line via an unidirectional conducting device; and

a charge pump for each electrostatic bus line to precharge its associated electrostatic bus line to an associated predetermined voltage level, wherein pre-charging each electrostatic bus line to its predetermined voltage level reduces transient currents on the signal bonding pads associated with capacitive charging of the electrostatic bus lines when the external voltage signal levels are beyond normal supply voltage ranges.

2. The electrostatic discharge protection circuit of claim 1, wherein each electrostatic bus line is pre-charged to a voltage level beyond a normal supply voltage range.

3. The electrostatic discharge protection circuit of claim 1, wherein each charge pump comprises:

a first capacitor having a first plate and a second plate;

a second capacitor having a first plate and a second plate, the first plate of the second capacitor is coupled to an electrostatic bus line, the second plate of the second capacitor is coupled to a first bonding pad and a first polarity terminal of a power supply;

a first switch having a first position and a second position, wherein when the first switch is in the first position the first plate of the first capacitor is coupled to the

first polarity terminal of the power source, the second plate of the second capacitor and the first bonding pad, further wherein when the first switch is positioned in the second position the first plate of the first capacitor is coupled to the first plate of the second capacitor and the electrostatic bus line; and

a second switch having a first position and a second position, wherein when the second switch is in the first position the second plate of the first capacitor is coupled to a second polarity terminal of a power supply and a second bonding pad, further wherein when the second switch is in the second position the second plate of the first capacitor is coupled to the first polarity terminal of the power supply, the second plate of the second capacitor and the first bonding pad.

4. The electrostatic discharge protection circuit of claim 1, wherein each unidirectional conducting device comprises:

a steering diode coupled to steer the electrostatic discharge away from the internal circuitry, wherein the pre-charging of an associated electrostatic bus line causes the steering diode to remain reversed biased even if voltages on associated signal bonding pads are beyond the normal supply voltage range and below a predetermined voltage range.

5. The electrostatic discharge protection device of claim 4, wherein the steering diode is a rectifier diode.

6. The electrostatic discharge protection device of claim 4, wherein the steering diode is a Schottky diode.

7. The electrostatic discharge protection device of claim 1, wherein each unidirectional conducting device comprises:

a junction of a bipolar junction transistor.

8. The electrostatic discharge protection device of claim 7, wherein the bipolar junction transistor is formed with in a complementary metal-oxide semiconductor (CMOS) N well structure.

9. The electrostatic discharge protection device of claim 7, wherein the bipolar junction transistor is formed in a CMOS P well structure.

10. The electrostatic discharge protection device of claim 1, further comprising:

a switching device coupled to each electrostatic bus line to selectively pass electrostatic pulses from one of the bonding pads to another of the bonding pads.

11. The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

a bipolar junction transistor coupled to switch in response to the electrostatic pulses.

12. The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

a MOSFET coupled to switch in response to the electrostatic pulses.

13. The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

a zener diode.

14. An integrated circuit comprising:

functional circuitry;

a first electrostatic discharge (ESD) bus line to direct electrostatic discharge pulses away from the functional circuitry;

a first charge pump coupled to charge the first ESD bus line to a predetermined first voltage;

a second ESD bus line to further direct electrostatic discharge pulses away from the functional circuitry;

a second charge pump coupled to charge the second ESD bus line to a predetermined second voltage;

a first unidirectional conducting device coupled between a first signal connection and the first ESD bus line;

a second unidirectional conducting device coupled between a second signal connection and the second ESD bus line; and

wherein the first and second ESD bus lines are charged to their respective first and second voltage levels to reduce transient currents through the first and second unidirectional conducting devices when voltages applied to the first and second signal connections are outside the normal range of power supply operating voltages for the integrated circuit.

15. The integrated circuit of claim 14, wherein the first unidirectional conducting device is a diode having a cathode terminal coupled to the first ESD bus line and an anode terminal coupled to the first signal connection.

16. The integrated circuit of claim 14, wherein the second unidirectional conducting device is a diode having a cathode terminal coupled to the second signal connection and an anode terminal coupled to the second ESD bus line.

17. The integrated circuit of claim 14, wherein the first unidirectional conducting device comprises a pn junction wherein the N type material is coupled to the first ESD bus line and the P type material is coupled to the first signal connection, further wherein the second unidirectional device comprises pn material wherein the N type material is

coupled to the second signal connection and the P type material is coupled to the second ESD bus line.

18. The integrated circuit of claim 14, wherein the first voltage is a positive voltage with respect to a positive terminal of a power supply to the integrated circuit and the second voltage is a negative voltage with respect to a negative terminal of the power supply.

19. The integrated circuit of claim 14, wherein the first voltage is greater than an expected positive signal input voltage provided to the integrated circuit, further wherein the second voltage is less than a negative expected signal input voltage provided to the integrated circuit.

20. The electrostatic discharge protection circuit of claim 14, wherein the first charge pump comprises:

a first capacitor having a first plate and a second plate;

a second capacitor having a first plate and a second plate, the first plate of the second capacitor is coupled to the first ESD bus line, the second plate of the second capacitor is coupled to a first bonding pad and a first polarity terminal of a power supply;

a first switch having a first position and a second position, wherein when the first switch is in the first position the first plate of the first capacitor is coupled to the first polarity terminal of the power source, the second plate of the second capacitor and the first bonding pad, further wherein when the first switch is positioned in the second position the first plate of the first capacitor is coupled to the first plate of the second capacitor and the first ESD bus line; and

a second switch having a first position and a second position, wherein when the second switch is in the first position the second plate of the first capacitor is coupled to a second polarity terminal of a power supply and a second bonding pad, further wherein

when the second switch is in the second position the second plate of the first capacitor is coupled to the first polarity terminal of the power supply, the second plate of the second capacitor and the first bonding pad.

21. The electrostatic discharge protection circuit of claim 14, wherein the second charge pump comprises:

a first capacitor having a first plate and a second plate;

a second capacitor having a first plate and a second plate, the first plate of the second capacitor is coupled to second ESD bus line, the second plate of the second capacitor is coupled to a first bonding pad and a first polarity terminal of a power supply;

a first switch having a first position and a second position, wherein when the first switch is in the first position the first plate of the first capacitor is coupled to the first polarity terminal of the power source, the second plate of the second capacitor and the first bonding pad, further wherein when the first switch is positioned in the second position the first plate of the first capacitor is coupled to the first plate of the second capacitor and the second ESD bus line; and

a second switch having a first position and a second position, wherein when the second switch is in the first position the second plate of the first capacitor is coupled to a second polarity terminal of a power supply and a second bonding pad, further wherein when the second switch is in the second position the second plate of the first capacitor is coupled to the first polarity terminal of the power supply, the second plate of the second capacitor and the first bonding pad.

22. The integrated circuit of claim 14, further comprising:

a switching device coupled between the first and second ESD bus lines, the switching device is switchable between a high impedance and low impedance state.

23. The integrated circuit of claim 22, wherein when a voltage pulse greater than a predetermined third voltage is applied between the first and second ESD bus lines, the switching device closes and conducts such that the resulting current is steered from the first ESD bus line and through the switching device to the second ESD bus line thereby limiting the voltage pulse and routing the resulting current pulse away from functional circuitry of the integrated circuit.

24. The integrated circuit of claim 22, wherein the switching device further comprises:

a capacitor;

a resistor, the capacitor and resistor are coupled in series between the first and second ESD bus lines, wherein the capacitor is coupled to the first ESD bus line and the resistor is coupled to the second ESD bus line; and

a transistor, the transistor having a collector coupled to the first ESD bus line and an emitter coupled to the second ESD bus line, the transistor further having a base coupled to a connection between the capacitor and the resistor.

25. The integrated circuit of claim 22, wherein the switching device further comprises:

a zener diode;

a resistor, the zener diode and resistor are coupled in series between the first and second ESD bus lines, wherein an anode of the zener diode is coupled to the first ESD bus line and the resistor is coupled to the second ESD bus line; and

a transistor, the transistor having a collector coupled to the first ESD bus line and an emitter coupled to the second ESD bus line, the transistor further having a base coupled to a connection between a cathode of the zener diode and the resistor.

26. An ESD protected integrated circuit comprising:

a positive ESD bus line to route positive electrostatic discharge pulses around functional circuitry;

first and second signal bonding pads to receive external voltage signals;

a first unidirectional conducting device coupled between the first signal bonding pad and the positive ESD bus line;

a second bus line coupled to selectively receive current from the positive ESD bus line;

a second unidirectional conducting device coupled between the second signal bonding pad and the second bus line; and

a positive rail charge pump coupled to charge the positive ESD bus line to a predefined voltage level, wherein the predefined voltage level is higher than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting device during normal operations of the integrated circuit where voltage signals higher than a normal power supply operating voltage, but less than the predefined voltage, are applied to the first signal bonding pad.

27. The ESD protected integrated circuit of claim 26, wherein the second unidirectional conducting device comprises a diode.

28. The ESD protected integrated circuit of claim 26, further comprising:

a supply clamp to selectively conduct current from the positive ESD bus line to the second bus line when a positive electrostatic discharge pulse is detected, the supply clamp is coupled between the positive ESD bus line and the second bus line.

29. The ESD protected integrated circuit of claim 26, wherein each of the first and second unidirectional conducting devices comprise a diode.

30. The ESD protected integrated circuit of claim 29, wherein the predefined voltage level keeps the diodes in a reverse bias state during normal operation.

31. The ESD protected integrated circuit of claim 26, wherein the first unidirectional conducting device comprises a transistor.

32. The ESD protected integrated circuit of claim 31, wherein a base terminal of the transistor is coupled to the positive ESD bus line and the collector emitter path of the first transistor is coupled between the first signal bonding pad and a first input of a Vss pad, further wherein the Vss pad is used to couple a negative supply voltage to the second bus line.

33. The ESD protected integrated circuit of claim 31, wherein the transistor is formed in a N well CMOS structure.

34. The ESD protection integrated circuit of claim 33, wherein the N well CMOS structure further comprises:

a N type conductivity well formed in a P type conductivity substrate of the integrated circuit;

a N type conductivity base formed by the well;

a P type conductivity emitter with high dopant density formed in the well; and

a P type conductivity collector formed by the substrate.

35. The ESD protection integrated circuit of claim 34, further comprising:

a diode coupled between the first signal pad and the second bus line, the diode having a N type conductivity cathode with high dopant density formed in the P type conductivity substrate.

36. An ESD protected integrated circuit comprising:

a negative ESD bus line to route negative electrostatic discharge pulses around functional circuitry;

first and second signal bonding pads to receive external voltage signals;

a first unidirectional conducting device coupled between the first signal bonding pad and the negative ESD bus line;

a second bus line coupled to selectively receive current from the negative ESD bus line;

a second unidirectional conducting device coupled between the second signal bonding pad and the second bus line; and

a negative rail charge pump coupled to charge the negative ESD bus line to a predefined voltage level, wherein the predefined voltage level is lower than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting devices during normal operations of the integrated circuit where voltage signals lower than a normal power supply operating voltage, but more than the predefined voltage, are applied to the first signal bonding pad.

37. The ESD protected integrated circuit of claim 36, wherein the second unidirectional conducting device comprises a diode.

38. The ESD protected integrated circuit of claim 36, further comprising:

a supply clamp to selectively conduct current from the negative ESD bus line to the second bus line when a negative electrostatic discharge pulse is detected, the supply clamp is coupled between the negative ESD bus line and the second bus line.

39. The ESD protected integrated circuit of claim 36, wherein each of the first and second unidirectional conducting devices comprise a diode.

40. The ESD protected integrated circuit of claim 39, wherein the predefined voltage level keeps the diodes in a reverse bias state during normal operation.

41. The ESD protected integrated circuit of claim 36, wherein the first unidirectional conducting device comprises a transistor.

42. The ESD protected integrated circuit of claim 41, wherein a base terminal of the transistor is coupled to the negative ESD bus line and the collector/emitter path of the first transistor is coupled between the first signal bonding pad and a first input of a Vdd pad, further wherein the Vdd pad is used to couple a positive supply voltage to the second bus line.

43. The ESD protected integrated circuit of claim 41, wherein the transistor is formed in a P well CMOS structure.

44. The ESD protection integrated circuit of claim 43, wherein the P well CMOS structure further comprises:

a P type conductivity well formed in a N type conductivity substrate of the integrated circuit;

a P type conductivity base formed by the well;

a N type conductivity emitter with high dopant density formed in the well; and

a N type conductivity collector formed by the substrate.

45. The ESD protection integrated circuit of claim 44, further comprising:

a diode coupled between the first signal pad and the second bus line, the diode having a P type conductivity anode with high dopant density formed in the N type conductivity substrate.

46. A method of operating an integrated circuit that requires signal voltages outside the normal range of operational power supply voltages, the integrated circuit including an electrostatic discharge circuit having one or more electrostatic discharge bus lines, the method comprising:

pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.

47. The method of claim 46, wherein pre-charging the electrostatic discharge bus lines prevents parasitic current from flowing through unidirectional conducting devices when signal voltages are applied to the integrated circuit that are outside the normal range of operating power supply voltages during operation of the integrated circuit.

48. The method of claim 46, wherein an electrostatic bus line is pre-charged to a voltage level higher than an expected positive voltage signal.

49. The method of claim 46, wherein an electrostatic bus line is pre-charged to a voltage level lower than an expected negative voltage signal.

50. A method of operating an integrated circuit having electrostatic discharge protection comprising:

coupling a positive ESD bus line to the integrated circuit to direct positive electrostatic pulses away from functional circuitry of the integrate circuit;

pre-charging the positive ESD bus line to a predetermined positive voltage level, wherein the predetermined positive voltage level is above a voltage level of expected signals to be applied to the integrated circuit;

coupling a negative ESD bus line to the integrated circuit to direct negative electrostatic pulses away from the functional circuitry of the integrated circuit; and

pre-charging the negative ESD bus line to a predetermined negative voltage level, wherein the predetermined negative voltage level is below the voltage level of expected signals to be applied to the integrated circuit.

51. The method of claim 50, further comprising:

limiting the voltage between the positive and negative ESD bus lines with a supply clamp.

52. The method of claim 50, further comprising:

coupling one more unidirectional conductors between the positive ESD bus line and one or more signal connections to direct electrostatic pulses away from the functional circuitry, wherein the pre-charging of the positive ESD bus line to the predetermined positive voltage level reduces parasitic currents through unidirectional conductors during normal operations of the integrated circuit.

53. The method of claim 50, further comprising:

coupling one more unidirectional conductors between the negative ESD bus line and one or more signal connections to direct electrostatic pulses away from the functional circuitry, wherein the pre-charging of the negative ESD bus line to the predetermined negative voltage level reduces parasitic currents through unidirectional conductors during normal operations of the integrated circuit.

54. The method of claim 50, wherein the positive ESD bus line is pre-charged to a voltage level above the positive supply voltage Vdd.

55. The method of claim 54, wherein pre-charging the positive ESD bus line minimizes parasitic currents through unidirectional conducting devices when operating signals are applied to he integrated circuit that having voltage levels above Vdd but less than the predetermined positive voltage level.

56. The method of claim 50, wherein the negative ESD bus line is pre-charged to a voltage level below the negative supply voltage Vss.

57. The method of claim 56, wherein pre-charging the negative ESD bus line minimizes parasitic currents through unidirectional conducting devices when operating signals are applied to he integrated circuit that having voltage levels below Vss but higher than the predetermined negative voltage level.